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Voltage-Controlled Oscillator in the Coil

Frank Zhang, Chen-Feng Chu, and Peter Kinget

Department of Electrical Engineering
Columbia University, New York, NY 10027 U.S.A.

Abstract— **In this paper we have examined the effect of devices inside an inductor through simulations and measurements. A voltage-controlled oscillator (VCO) was constructed inside an inductor using layout techniques that minimize eddy current loss and magnetic coupling. Measurement results show that this compact VCO has an equal performance in phase noise and output power as compared to a traditional VCO while reducing the area by about** 50%**.**

I. Introduction

Spiral on-chip inductors often occupy more than half of the total chip area in many radio frequency integrated circuits (RFICs). The region in and around the inductor is typically kept clear of active and passive devices to avoid the generation of eddy current in these devices, which degrades the quality factor, Q, of the inductor. However, if the size of the close-by devices is kept small, the induced eddy current loops are localized in small regions which keeps the losses to a minimum. Furthermore, by carefully planning the current paths of the devices, magnetic coupling between the device currents and the inductor currents can be reduced. With these two properties in mind, we explore the possibility of placing active and passive devices under an on-chip inductor, to reduce the area and the cost of RFICs. We first investigate the effect of metal fills placed in and around the inductor on its Q using electro-magnetic (EM) simulations and measurements on test-structures. Since VCO phase noise is very sensitive to the Q of the inductors, we then used two identically designed VCOs but with different layouts to verify the proposed "circuit-in-the-coil" concept. The "VCO-in-the-coil" has a VCO tank layout which places the transistors and varactors under the inductor, but avoids any significant additional losses. Comparison between the experimental results for this compact VCO and a VCO with a standard layout, demonstrate the effectiveness of the proposed approach.

II. Metal Fill Test Structures

The idea of utilizing the area under an inductor sprout from the practical consideration of metal density requirement. On-chip inductors are large, but they are often made of only two metal layers. Placing metal fills inside or near the inductor increases the metal density count but has the possible drawback of decreasing the Q of the inductor, through eddy current loss. Measurement results of inductors with metal fills have been reported before [1], [2], but none have established a relationship between fill cell size and inductor Q. This relationship is of great interest to this work since it allows us to estimate the largest device that can be placed inside an inductor.

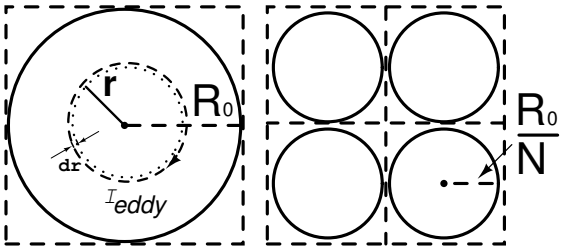

Fig. 1. Eddy current loss in metal fills.

Fig. 1 illustrates a thought experiment demonstrating eddy current in metal fills inside a magnetic field. Since we are mainly interested in the effect of metal fill structures with small dimensions which introduce minimal extra losses, we assume that the skin effect in the metal fill and the effect of the induced currents on the magnetic field can be neglected. The large circular metal fill in Fig. 1 has a radius R_0, and occupies about the same amount of area as four smaller circular metal fills with radius R_0/N, where N=2 in this case. For mathematical convenience, we use circular metal fills to approximate square metal fills used in real layouts. Assuming a small fill cell size compared to the dimensions of the inductor, the magnetic field, B, is uniform over the area of the metal fill cell, and is not a function of radius, r. The magnetic flux, Φ, enclosed in a circular loop of radius, r, is given by [3]:

$$\Phi = \oint B \cdot dA = B \cdot (\pi r^2). \tag{1}$$

Using Faraday's Law,

$$V = -\frac{d\Phi}{dt} = -\frac{dB}{dt} \cdot \pi r^2, \tag{2}$$

where V is the potential developed along any current path as a result of changing flux induced by the AC current in the inductor. The negative sign indicates that the current, I_{eddy}, induced by V, will flow in such a direction as to oppose the flux that produced it. The resistance, R, of a thin cylindrical sheet of metal fill, bounded by the dashed and dotted lines in Fig. 1 is equal to:

$$R = \frac{\rho}{h \cdot dr} \cdot (2\pi r), \tag{3}$$

where ρ is the resistivity of the fill metal, h is the height of the metal fill, and dr is the incremental thickness of the cylindrical sheet. From Eq. (2) and (3), the total power dissipated in a

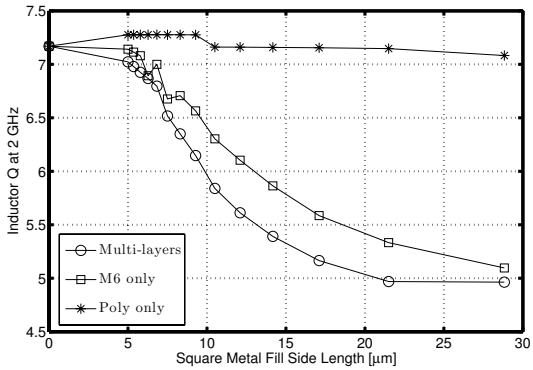

Fig. 2. Simulated inductor Q from EM simulator for different metal fill cell sizes and resistivity. Metal fill side length of zero represents the case where no metal fills were used.

metal fill with radius, R_0, is:

$$P_{\text{diss}} = \int \frac{V^2}{R} = \int_0^{R_0} \left(\frac{dB}{dt}\right)^2 \cdot \frac{\pi \cdot h}{2 \cdot \rho} \cdot r^3 dr. \tag{4}$$

Since a large metal fill can be replaced by N^2 small metal fills, the power dissipation for the two cases are:

$$P_{\text{diss}} = \begin{cases} \left(\frac{dB}{dt}\right)^2 \cdot \frac{\pi \cdot h}{8 \cdot \rho} \cdot R_0^4 & \text{(large fill)} \\ \left(\frac{dB}{dt}\right)^2 \cdot \frac{\pi \cdot h}{8 \cdot \rho} \cdot \frac{R_0^4}{N^2} & \text{(small fill)} \end{cases} \tag{5}$$

The power dissipated in the metal fills is an additional loss mechanism for the inductor and thus reduces its Q. However, Eq. (5) illustrates that this extra loss can be significantly reduced by using metal fills with small fill cell sizes. Eq. (5) provides guidelines on device sizing inside an inductor but is not sufficiently accurate for quantitative estimates. We ran extensive full-wave simulations on inductors with different fill cell sizes using the EM simulator EMX [4]. Fig. 2 shows the simulated Q at 2 GHz of a five-turn, 4.5 nH differential inductor, L_{diff}, for different fill cell sizes and resistivity. L_{diff} is used in the VCO in Fig. 5, which will be described later. The inductor is constructed using the thick top metal, and has an outer diameter of 200 μm, inner diameter of 80 μm, trace width of 10 μm, and a trace spacing of 3 μm. The metal fills are constructed by stacking all the available metal and polysilicon layers without vias in between, and they are placed in the center of the inductor. The Q degrades rapidly as the metal fill dimensions become large, however, for the more resistive polysilicon fills, the eddy loss is much less, as predicted by Eq. (5).

The accuracy of EMX simulation was compared against measurement data from test structures in a 0.25 μm BiCMOS process. The die photo of the test structures is shown in Fig. 3. A single-ended 2.3 nH inductor was constructed using the thick top metal layer, with an outer diameter of 200 μm, an inner diameter of 100 μm, a trace width of 10 μm, and a trace spacing of 3 μm. The metal fills were 7 μm–by–7 μm squares with a spacing of 3 μm, and were of the multi-layer type. The metal fills were placed both inside and around the inductor. A small error of less than 5% in Q was observed

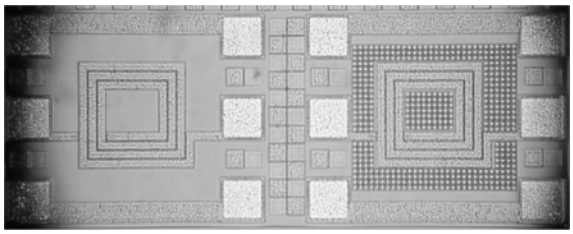

Fig. 3. Die photo of the metal fill test structures: plain inductor (left), with metal fills (right).

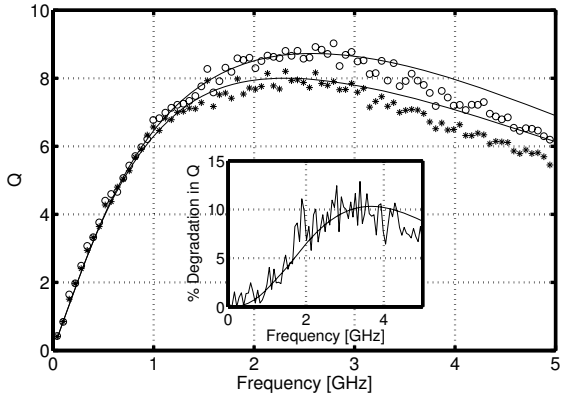

Fig. 4. Eddy current loss with respect to metal fill area. Inset: Percentage degradation in Q with respect to frequency.

between the simulated and the measured data below 3 GHz. A maximum Q degradation of $\sim 10\%$ occurs at its peak, similar to results reported in [1], [2]. The typical application range of an inductor in a tunable VCO is below its peak Q frequency since the varactors and the parasitics of the active devices add significantly to the tank capacitance [5].

III. VCO IN THE COIL

To develop a compact VCO layout we studied the placement of varactors inside and under the inductor. We first modified the layout of the differential inductor, L_{diff}, to allow placement of the varactors inside the inductor. By folding the leads of the inductor "outside in," the cathodes of the varactors can be connected along the inner-most turn of the inductor, as shown in Fig. 6. Although this connection can result in a distributed effect, which is undesirable in a narrowband circuit, the actual effect on the circuit was small since the inner-most turn only contributes to a small fraction of the total inductance. A simulation using a distributed model for the inner section of the inductor, connected to varactors, confirmed that the distributed effect was indeed negligible. Thus, the varactors were connected as shown in Fig. 5 for circuit simulations.

Next, we considered the layout options for the V_{tune} line that connects the anodes of the varactors together. We compared two possible configurations for the V_{tune} line, shown in Fig. 6. In Fig. 6a, the anode of the varactors are connected together on the outside of the inductor. The drawback of this configuration is that the current paths of the V_{tune} line are parallel to the flow of the inductor current, causing further unwanted magnetic coupling. The configuration shown in Fig. 6b distributes the V_{tune} line from the center of the

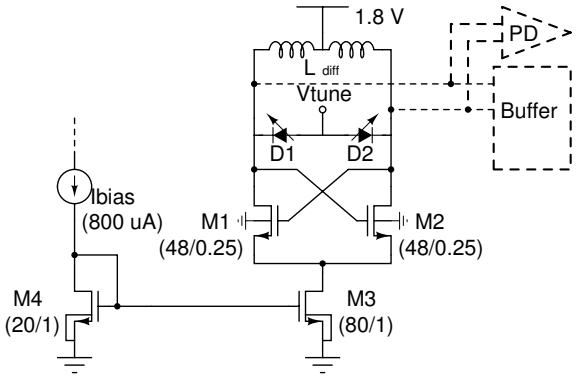

Fig. 5. Schematic for the "VCO-in-the-coil" and regular VCO; the Buffer and peak detector (PD) are auxiliary circuits to facilitate the measurements.

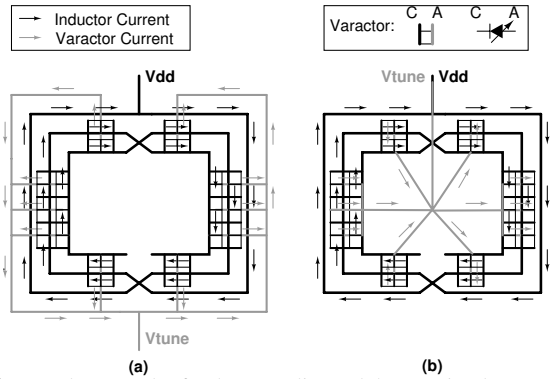

Fig. 6. Two layout styles for the V_{tune} line and the associated current flows.

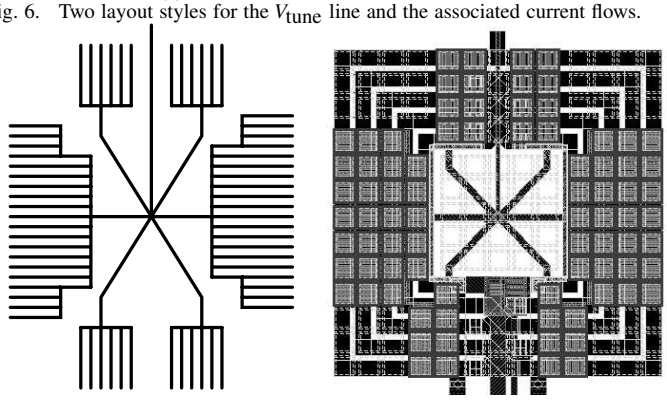

Fig. 7. Rake-shaped V_{tune} line and the "VCO-in-the-coil" layout.

inductor, thus keeping the wires with parallel current flow far apart. Fig. 7a shows the details of the rake-shaped metal wiring used to connect the anodes of the varactors. The shape of the wiring is similar to that of a patterned ground shield (PGS) [6]. The fingers of the rake-shaped wiring are oriented such that the current flow in them is perpendicular to the direction of the inductor current, thus minimizing magnetic coupling between the two. Furthermore, since the V_{tune} node in Fig. 5 is a signal ground for differential signals, the rake-shaped wiring acts as a grounded PGS which absorbs any stray electric field from the inductor to the substrate, thus improving the Q of the inductor [6].

Another important concern in the VCO tank layout is the resistance of the V_{tune} line, since its series resistance adds thermal noise which is directly upconverted into phase noise [5]. Parasitic resistance extraction was performed on the longest wire path from the V_{tune} pin to the varactor anode. From simulation, the lowest series resistance tolerable for the phase noise requirement was calculated. In order to lower the wire resistance, multiple metal layers were strapped together. Lowering the resistance of the V_{tune} line worsens its eddy current effect on the inductor, as Eq. (5) suggests. However, the rake-shaped wiring in Fig. 7a prevents eddy currents from circulating in large loops, thus minimizing their effect.

Fig. 7b shows the complete layout of the VCO. We first simulated the differential inductor, L_{diff}, by itself using EMX, and found a quality factor of about 7 at 2 GHz. Next, 82 small varactors of dimensions 12 μm–by–11 μm, collectively shown as D1 and D2 in Fig. 5, were connected to the differential inductor. The varactor diodes D1 and D2 are made from p+ base in the nwell and have a simulated Q of about 40 at 2 GHz. Unlike metal fills, varactors actively participate in the circuit operation and carry AC currents. Their effect on the inductor is thus potentially more complicated than just extra loss due to eddy currents. However, it is not possible to conduct EM simulations that include active circuit and varactor device behavior. For the EMX simulations, the varactors were replaced with parallel plate capacitors with similar plate resistivity as the varactor diodes while keeping the wiring same. Simulations showed that the Q degradation is minimal when the varactors are placed under the inductor traces instead of at the center of the inductor. Not only are they exposed to a smaller magnetic field there, but they also perform the role of a PGS by further isolating the inductor from the lossy substrate. The active devices, which include a cross-coupled pair, current source, and current mirror were placed at the bottom center of the inductor. We ran EMX simulation on the entire VCO structure which includes the differential inductor, the rake-shaped multi-layer metal routing, the parallel plate capacitors used to model the varactors, and the active devices. The extracted inductor S-parameters, which include all the eddy current effects were used to evaluate the VCO in circuit simulations. Simulation results confirmed that the performance of the compact VCO is very close to the performance of the VCO with a plain inductor.

Two VCOs were constructed—the "VCO-in-the-coil" with varactors and actives inside the inductor, henceforth referred to as "VCO IN", and a regular VCO with varactors and actives outside the inductor, henceforth referred to as "VCO OUT". The VCOs were implemented in a 0.25 μm BiCMOS process with only the peak detector implemented in bipolar. Both VCOs, shown in Fig. 11, consume 3.2 mA from a 1.8 V supply. The VCO output is connected to a buffer stage as well as a peak detector running off a 2.5 V supply.

Four sets of VCOs were characterized with a Cascade RF probe station and an Agilent E4446A spectrum analyzer; the measured data was very consistent and the results of a typical set are shown in Figs. 8-10. Fig. 8a shows the tuning characteristic of the VCOs; a very wide tuning range of 520 MHz, or 26 % of the center frequency was achieved.

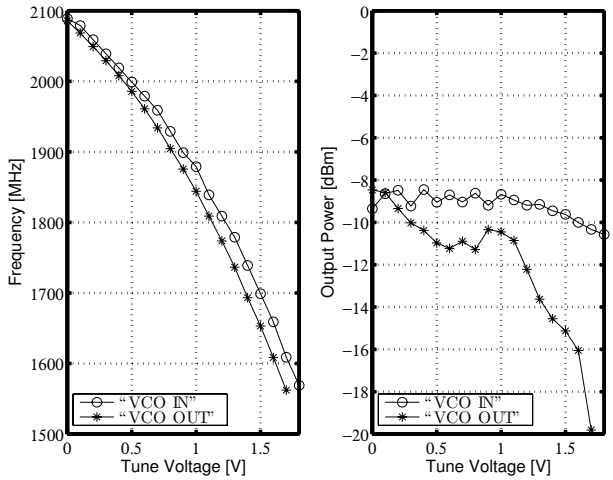

Fig. 8. Measured tuning characteristic of the VCOs.

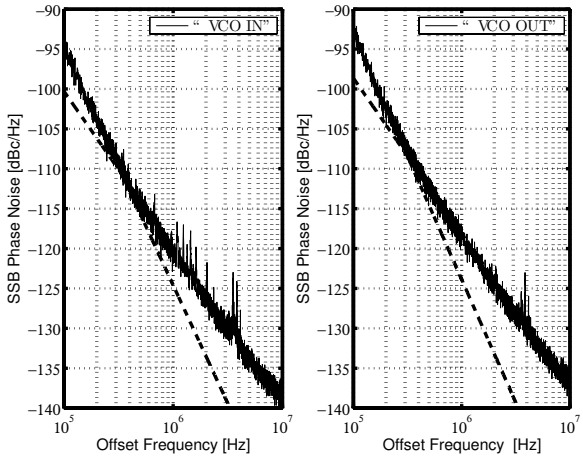

Fig. 9. Measured phase noise spectrum for a 2 GHz carrier frequency; the dashed lines have a $1/f^2$ and $1/f^3$ slope, the corner frequency is ~ 300 kHz.

Fig. 8b shows the output power for different tune voltages. Both oscillators have a similar output power except for high tune voltages, which corresponds to low output frequencies. We currently do not have a conclusive explanation for the higher output power from "VCO IN" and the reduction of output power in "VCO OUT". Fig. 9 shows the noise spectrum of the VCOs and Fig. 10 shows the variation in phase noise for different tuning voltages at various offset frequencies. The two VCOs have close to identical performance.

Returning to the die photo of the VCOs in Fig. 11, "VCO OUT" on the right occupies 0.3×0.25 mm^2, and "VCO IN" on the left occupies 0.2×0.2 mm^2, resulting in an area saving of 47%.

IV. Conclusions

We have shown through experiments and simulations that eddy current loss accounts for the majority of the degradation in quality factor when devices are placed inside the inductor. However, by breaking the devices into smaller pieces, the eddy current loops are localized and therefore the resistive loss is minimized. Using this technique, a large number of varactors as well as active devices are placed inside an inductor to create

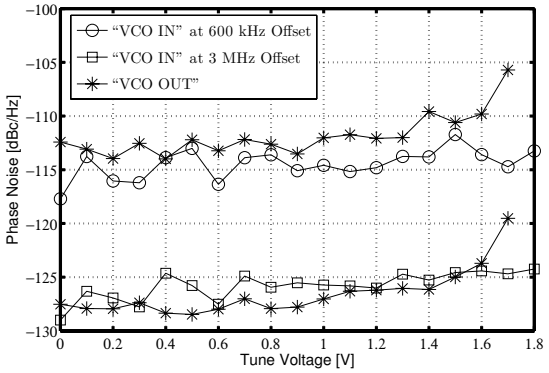

Fig. 10. Measured phase noise for different tune voltages.

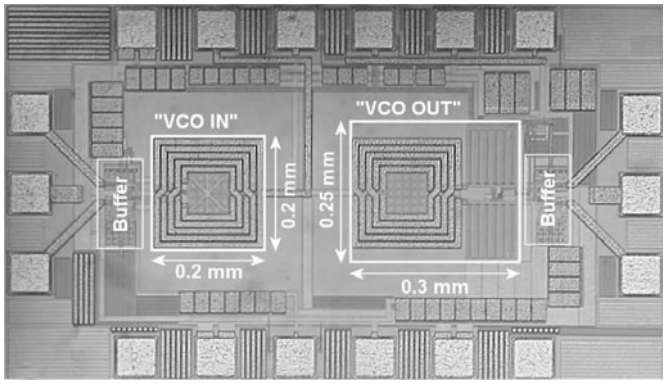

Fig. 11. VCO die photo.

a compact VCO that has equal performance as a traditional VCO. The "VCO-in-the-coil" fits completely inside the area of the tank inductor. This circuit-in-the-coil technique can be easily extended to other applications, e.g., the capacitors of a PLL loop filter can be placed under the VCO inductor to save area.

V. Acknowledgments

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